IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	M. H. McKerreghan et al.	Date:	March 16, 2009
Application No.:	10/536,859	Examiner:	N.W. Ha
Filing Date:	June 26, 2006	Group Art Unit:	2814
Title:	PACKAGE HAVING EXPOSE INTEGRATED CIRCUIT DEVICE		

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

An Information Disclosure Statement under 37 C.F.R. §§ 1.97 and 1.98 is submitted herewith. The Examiner's attention is respectfully directed to the U.S. Patent and foreign patent document listed on the enclosed form PTO/SB/08.

The documents listed herein were cited in an office action in a counterpart foreign application. Applicants' undersigned attorney will provide a copy of the foreign patent document as soon as it is available.

CERTIFICATE OF MAILING OR TRANSMISSION (37 C.F.R. § 1.8(a))

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being:

☐ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (571) 273-8300.

☒ transmitted via the electronic filing system of the United States Patent and Trademark Office on the date shown below and in accordance with 37 C.F.R. § 1.6(a)(4).

March 16, 2009 Signed: Brenda Musco

Brenda Musco

It is noted that the cited foreign patent document is not in the English language. A concise explanation of the relevance of this reference is as follows: The reference describes a process including providing a semiconductor wafer, wherein a plurality of chips are formed thereon and a plurality of bonding pads are formed on the central area of the chip; cutting adjacent chips so as to form a recess on the edge of a second surface and a recess on the edge of a first surface of each chip; cutting the wafer so as to form a plurality of single chips; forming a solder on each bonding pad; and encapsulating the chip and the recesses with resin.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(d).

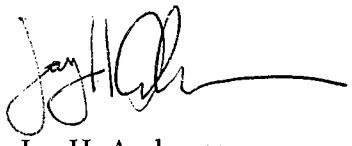
Statement under 37 C.F.R. § 1.97(e)(1)

Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

The Commissioner is authorized to charge $180.00 to cover the required fee under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-1665. Any deficiency in or overpayment of this fee, or any other required fee, should likewise be charged or credited to Deposit Account No. 23-1665.

The applicants' undersigned attorney may be reached by telephone at 212-551-2625. All correspondence should continue to be directed to the address given below, which is the address associated with Customer Number 27267.

Respectfully submitted,



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